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Interface optimization using diindenoperylene for C_{60} thin film transistors with high electron mobility and stability

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ABSTRACT

C_{60}-based organic thin film transistors (OTFTs) with high electron mobility and high operational stability are achieved with (1 1 1) oriented C_{60} films grown by using template effects of diindenoperylene (DIP) under layer on the SiO_2 gate insulator. The electron mobility of the C_{60} transistor is significantly increased from 0.21 $cm^2 V^{-1} s^{-1}$ to 2.92 $cm^2 V^{-1} s^{-1}$ by inserting the template-DIP layer. Moreover much higher operational stability is also observed for the DIP-template C_{60} OTFTs. A grazing incidence X-ray diffraction and ultra-high-sensitivity photoelectron spectroscopy measurements indicate that the improved electron mobility and stability arise from the decreased density of trap states in the C_{60} film due to increased (1 1 1) orientation of C_{60}-grains and their crystallinity on the DIP template.

1. Introduction

Although organic devices have attracted great attention in the past decades because of their advantages in realizing low-cost, large-area and flexibility devices, the charge carrier mobility of active organic layer and the device stability are not sufficient and have been required to be increased [1–6]. Among various organic devices, performance of organic thin film transistors (OTFTs) is mainly dominated by the mobility, thus OTFTs have been utilized in studying origins of the poor mobility and in developing a technology for improving the mobility [7,8].

It has been known that the density of charge trap states in organic active layers is one of the key factors [9] that limit charge transport properties. Furthermore it has been also known that intermolecular interactions at the interface, which significantly affect the molecular orientation, packing structure and their electronic states, play a crucial role in the electron/hole transport characteristics [10–13]. To reduce the density of trap states in OFETs with SiO_2 gate insulator, which originates from hydroxyl groups on the SiO_2 surface [9], various organic films, such as self-assembled monolayer (SAM) modification of dielectric surfaces [14–17], and films of organic small molecules [10–12, 18–20], have been utilized to separate the active layer from the trap states at the SiO_2 surface and to reduce structural defects in the active over-layer films. Oriented single crystals grown by directional solution shearing processes have also been studied to use single crystal property of higher mobility instead of thin polycrystalline films

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[1,21]. Among these different methods, the thin organic inter layer could enhance the crystallinity of the organic active layer on top and improve its charge mobility [10–12]. It was shown, for example, that an interlayer of pentacene improved the structure of C_{60} film on top, which could increase the electron mobility (μ_n) by more than a factor of 5 in the C_{60} channel [10]. However, the large OFF drain current (I_{ds}), arising from the hole transport through pentacene, could limit the ON/OFF I_{ds} ratio of the C_{60} channel.

On the other hand, Hinderhofer et al. reported recently that diindenoperylene (DIP; Fig. 1a) could be used to grow highly ordered and oriented C_{60} films with its (1 1 1) plane parallel to the SiO_2 substrate [22–25]. They also demonstrated that growth of the well-oriented C_{60} film on DIP/SiO_2 is mediated by a template effect of the underlying DIP. It is expected that small OFF I_{ds} could be achieved by using DIP as template layer in C_{60}-based OTFTs because of the relatively low hole mobility of DIP single crystals (0.005 $cm^2 V^{-1} s^{-1}$ at room temperature [26]), Thus the C_{60}/DIP/SiO_2 structure may be an interesting choice for improving performance of n-type OTFTs.

In this work we demonstrate a dramatic μ_n improvement in C_{60}-based OTFTs using ultrathin DIP as a template layer. μ_n in the DIP-template C_{60} films can be as high as 2.92 $cm^2 V^{-1} s^{-1}$, which is more than tenfold higher than the reference device without the DIP template layer. The enhanced operational stability is also found for the DIP-template C_{60} OTFTs. The film morphology, structure and trap density characterizations by atomic force microscopy (AFM), grazing incidence X-ray diffraction (GIXD) and ultrahigh-sensitivity ultraviolet photoelectron spectroscopy (UPS), respectively, reveal that the ultrathin DIP template between the SiO_2 and C_{60} improves not only the crystallinity, crystal grain orientation and grain size of the C_{60} films, but also reduces significantly the density of trap states in the C_{60} films. Both effects contribute to the increase of μ_n and operational stability of the C_{60}-based OTFTs.

2. Experimental section

2.1. Device fabrication and characterization

The C_{60}-based OTFTs were fabricated on heavily p doped Si (100) substrates with 200-nm-thick thermal oxide (SiO_2) on the surface. After standard cleaning [27], the substrates were introduced into a molecule-deposition chamber with the base pressure of $\sim 2 \times 10^{-6}$ Torr. DIP with thickness of 3 nm was firstly vacuum deposited on the SiO_2 at a deposition rate of 0.1 nm/s. Then 30-nm-thick C_{60} was deposited on the top of DIP at a deposition rate of 0.1 nm/s. C_{60} films directly deposited on the SiO_2 were also prepared as reference. Finally, the C_{60}-based OTFTs with channel width (W) = 750 μm and channel length (L) = 50 μm were fabricated by depositing the Cu top electrodes. The molecular structures of DIP and C_{60} are shown in Fig. 1a. All films were deposited on substrates kept at room temperature (RT).

The electrical mobility measurements and bias stress measurements were carried out at RT in a high-vacuum (10^{-6} Torr) probe station (Lake Shore). Transistors are shortly exposed to N_2 in order to transfer to the probe station for measurements. μ_n is calculated from the saturation regime based on the following equation:

$$I_{ds} = \mu_n \frac{CW}{2L}(V_{gs} - V_T)^2$$

where C is the dielectric capacitance per unit area, V_{gs} is the gate bias and V_T is the threshold voltage. For calculation the electron mobility of C_{60} (30 nm)/DIP (3 nm)/SiO_2 (200 nm) OFET structure, we assume that DIP template can be regarded as a part of the dielectric layer due to small electron mobility of ~0.1 cm^2/V s [30] with the dielectric permittivity of ~4 (assumed according to pentacene [28]), and the compensation factor S could be given by:

$$S = C_{d+DIP}/C_d = 1/\left(1 + \frac{\varepsilon_d}{\varepsilon_{DIP}} \times \frac{d_{DIP}}{d_d}\right)$$

where d_{DIP} and d_d are the thicknesses of the DIP and SiO_2 dielectric layers respectively. ε_{DIP} and ε_d are the dielectric constants of the DIP and SiO_2, respectively. As the ε_d of SiO_2 is 3.9, which is similar to $d\varepsilon_{DIP}$, the compensation factor S is mainly determined by d_{DIP}/d_d to result in ~1, since $d_d \gg d_{DIP}$.

2.2. Structure characterization of films

In situ GIXD was performed at the X04SA beamline of the Swiss Light Source, Paul Scherrer Institut, Villigen, Switzerland (lambda = 0.10 nm). The films were evaporated on similarly prepared SiO_2/Si (100) substrates at

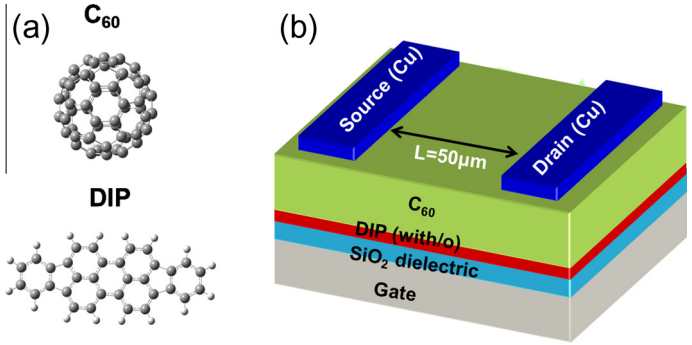

Fig. 1. (a) Molecular structures of C_{60} and DIP, and (b) schematic device structure of C_{60}-based OTFTs with or without DIP template layer.

RT. Lower limits of the in-plane coherent crystal sizes l_s were determined by the Scherrer formula:

$$I_s = 2\pi \times (\mathrm{FWHM})^{-1} \times 0.9394 \times K$$

where $K = 1.0747$ is the Scherrer constant for spherical grains and FWHM is the full width half maximum of the peak determined with a Gaussian fit-function. The instrumental broadening of the diffractometer was not included in the calculation; therefore only lower limits of l_s are given.

Surface morphology and roughness of similarly prepared C_{60} films on SiO_2 and DIP/SiO_2 were characterized by atomic force microscopy (AFM) (Vecco MultiMode V) at RT with a tapping mode.

2.3. Electronic structure characterization

The ultraviolet photoelectron spectroscopy (UPS) measurements were carried out in a vacuum pressure of 10^{-8} Pa by using ultrahigh sensitivity and low background apparatus with a hemispherical electron energy analyzer (MBS A-1) and a monochromatic Xe I ($h\nu = 8.437$ eV) radiation. More details about the ultrahigh sensitivity UPS can be found elsewhere [29]. All the films were evaporated on SiO_2/Si (1 0 0) at RT in the ultrahigh vacuum sample preparation chamber under a vacuum pressure of 10^{-7} Pa. The molecular deposition rates were similar to those for the transistor fabrication.

3. Results and discussion

3.1. Device characterization-influence of DIP modification

The device structure of the C_{60}-based OTFTs with or without DIP template layer is illustrated in Fig. 1b. Fig. 2a shows the bidirectional V_{gs}–I_{ds} transfer characteristics at a constant drain bias (V_{ds}) of 40 V with the V_{gs} sweep rate of 0.2 V/s. In Fig. 2a, the OTFT without DIP layer shows common n-type transistor behavior with relatively low μ_n of 0.21 $cm^2\ V^{-1}\ s^{-1}$. In contrast, upon inserting a template DIP layer between SiO_2 and C_{60}, high μ_n of 2.92 $cm^2\ V^{-1}\ s^{-1}$ is achieved, which is one order of magnitude higher than the reference device without DIP. Even compared with C_{60} grown on hexamethyldisilazane (HMDS)-modified SiO_2 substrate, which is about 0.32 cm^2/V s (not shown), more than 8 times higher μ_n is still achieved. Considering the poor electron mobility in the DIP layer, which is only 0.1 cm^2/V s [30], the drain-source current (I_{ds}) mostly flows in the C_{60} layer. Moreover, no p-type transistor behavior is found in the negative V_{gs} region, which is an advantage compared to C_{60}/pentacene OTFTs [10]. In addition, the threshold voltage V_T is reduced from 17 V to 5 V when using the DIP template layer, which is derived from the V_{gs}–$I_{ds}^{1/2}$ curves in the high V_{gs} region as shown in Fig. 2a. The I_{ds} ON/OFF ratio is 4×10^5 for the DIP template OTFT in contrast to 3×10^4 for the DIP-free one. All device parameters are summarized in Table 1. For DIP-template OTFTs, we did not observe noticeable V_{gs}-sweep-rate dependence of μ_n or threshold voltage [31]. The μ_n values are in the range of 2.62 ± 0.32 cm^2/V s for the V_{gs} sweep

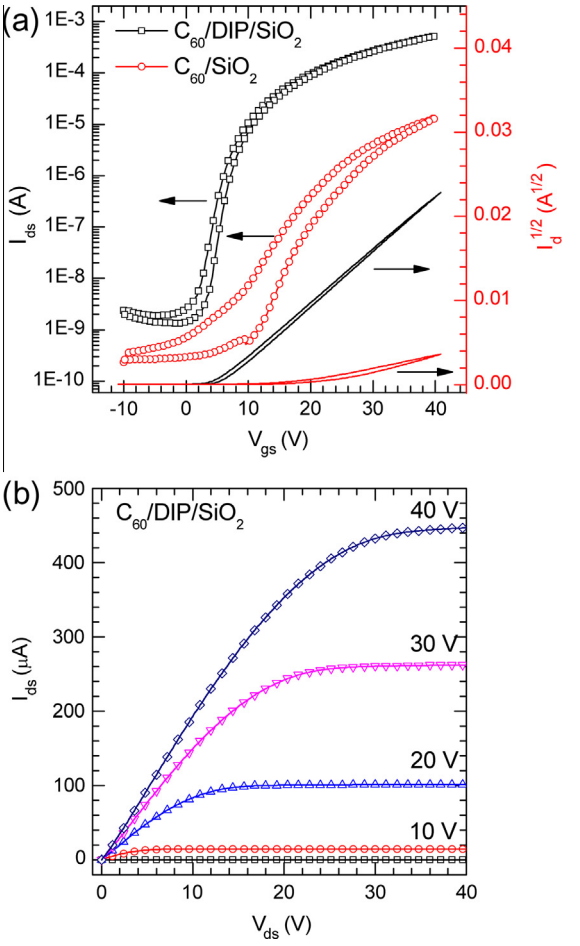

Fig. 2. (a) Bidirectional transfer characteristics of two C_{60}-based OTFTs (with and without DIP template layer) at $V_{ds} = 40$ V, where V_{gs}–$I_{ds}^{1/2}$ plots are also shown. (b) Output characteristics of a DIP-template C_{60}-based OTFT.

rates between 0.2 V/s and 1 V/s. Characteristics of the C_{60}-based OTFT with DIP layer, demonstrating good ohmic contact behavior in the low V_{ds} region and excellent I_{ds} saturation in the high V_{ds} region.

Operational stability of the C_{60}-based OTFTs with and without DIP template layer is also studied. Fig. 3 shows the normalized drain current as a function of time with bias stress of 40 V gate bias and 3 V drain bias under a vacuum pressure of 10^{-4} Pa. The C_{60} OTFT without DIP shows very rapid reduction of the drain current down to ~2% of the original current after 10^4 s, while the DIP-template C_{60} OTFT

Table 1
Summarized parameters of C_{60} transistors with and without DIP template layer.

Transistors	μ_n[a] ($cm^2\ V^{-1}\ s^{-1}$)	I_{ON}/I_{OFF}	V_T (V)
C_{60} with DIP	2.62 ± 0.32	4×10^5	5
C_{60} without DIP	0.21 ± 0.10	3×10^4	17

[a] The average mobilities with standard deviation were calculated from the results from 6 OFETs.

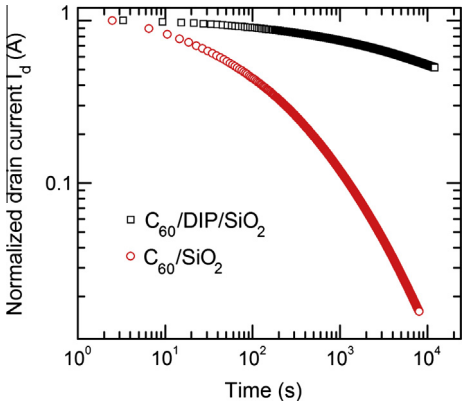

Fig. 3. Drain current in C_{60} based OTFTs with/o DIP template layer versus time taken at a gate and a drain voltage of 40 V and 3 V, respectively. The initial drain current was normalized to 1. The bias stress measurements were performed under the vacuum condition.

shows much higher stability with more than ~40-times improvement. Even after 10^4 s, the DIP-template C_{60} can still show half of the original drain current. With DIP template layer, the significant improvement in bias stress stability could be attributed to two effects. One is that the DIP inter-layer may suppress electron trapping at the surface and/or into the bulk of SiO_2. The other is that, the DIP template layer improves the ordering of C_{60} active layer and reduce density of trap states in the film, and consequently electron trapping within the n-channel is reduced as well. The latter is more effective since the HMDS-modified device does not show a dramatic increase in μ_n. The improved bias stress stability due to less trap states has also been reported on Rubrene single crystal [32].

3.2. Morphological and structural investigation

In order to understand the origin of the improved μ_n in the presence of DIP, the surface morphology of C_{60} deposited on SiO_2 and on DIP/SiO_2 is characterized by atomic force microscopy, as shown in Fig. 4. C_{60} films directly deposited on SiO_2 show smaller grain sizes with a root mean square (RMS) roughness of 0.91 nm (Fig. 4a). On the other hand the grain size of C_{60} films deposited on DIP/SiO_2 is increased to the RMS roughness of 1.31 nm (Fig. 4b). On the inset of Fig. 4, AFM line scans of the both samples are presented. Clearly, the C_{60} domain sizes are significantly larger on the DIP template as indicated by the distance between two deeper adjacent gaps marked by the red arrows in the line scans.

Clearer evidence of the increased domain size of C_{60} and its related ordered structure are observed from thickness dependent in-plane GIXD measurements during C_{60} evaporation. GIXD data from C_{60} films grown on SiO_2 and DIP/SiO_2 are shown in Fig. 5. At the bottom of each image, a GIXD scan at the final thickness (15 nm) are shown with peak assignments. In addition to a remarkable improvement of the C_{60} crystallinity on DIP/SiO_2 is seen from GIXD peak widths, note that peak assignments for both samples are different. This confirms that the C_{60} domains on DIP/SiO_2 are nearly completely oriented with the (1 1 1) plane parallel to the substrate surface in contrast to the randomly oriented C_{60} domains on SiO_2 as reported previously [23]. To a small degree, randomly oriented domains exist also in the C_{60} on DIP/SiO_2 as denoted by the (1 1 1)* reflection in Fig. 5b. From the peak widths at each thickness, the corresponding in-plane coherent island sizes l_s of both C_{60} films are calculated, and the results are shown in Fig. 6. It is clearly seen that even in the monolayer regime (~0.8 nm) l_s of C_{60} on DIP/SiO_2 is significantly larger than the l_s of C_{60} on SiO_2. This observation demonstrates that the crystallinity improvement of C_{60} is present from the very beginning of the film growth. For C_{60} thicknesses above 5 nm (~4 monolayers), the difference in l_s between both films stays nearly constant. Because of these observations, the superior performance of the DIP-template C_{60} OTFT is attributed at least to the increased crystallinity and (1 1 1) orientation of the C_{60} film on DIP, which is in favor of the electron transport in the C_{60} channel [27].

3.3. Direct measurements of trap states

The charge trap states are directly related to the band gap states produced mainly imperfectness of molecular packing structure. As pointed out previously [22], inserting a DIP template layer can reduce the density of gap states (DOGS) in the C_{60} film to result in a movement of the Fermi level (E_F) in the gap because of increased crystallinity of the C_{60} film structure. There are two major contributions of DOGS to the electrical conductivity: (i) contribution to the charge carrier concentration by change in the carrier injection through the interface (the energy level alignment issue) and (ii) contribution to the mobility by charge carrier trapping. Both of these depend on DOGS, which is mainly due to tailing of the lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) states into the band gap regions [22,29,33–36]. These DOGSs appear in principle through similar mechanism, but their values and energy distributions are not the same, respectively, because of the different spatial spreads of HOMO and LUMO [37] and different degeneracies of these states [34]. Depending on the deference of these DOGSs, the E_F may be located closer to the pristine LUMO or HOMO band, hence the transport type (p-, or n-type) is recognized by either high density of occupied gap states above HOMO (hole traps) or high density of unoccupied gap states below LUMO (electron traps). Thus quantitative measurements of DOGS of the C_{60} film with and without DIP template layer are indispensable to directly correlate the mobility, structure and electronic states.

Ultrahigh-sensitivity UPS is herein utilized to probe quantitatively the trap states (DOGS) above the HOMO of C_{60}, which is directly related to examine existence of the density of electron trap states below the LUMO. Fig. 7 shows the Xe I ($h\nu$ = 8.437 eV) UPS spectra of the C_{60} films (~15 nm) on SiO_2 and DIP/SiO_2. The background spectra of SiO_2 and DIP/SiO_2 are also shown as reference, since UPS spectra with Xe I radiation include both the signals from C_{60} as well as from the substrate due to large electron

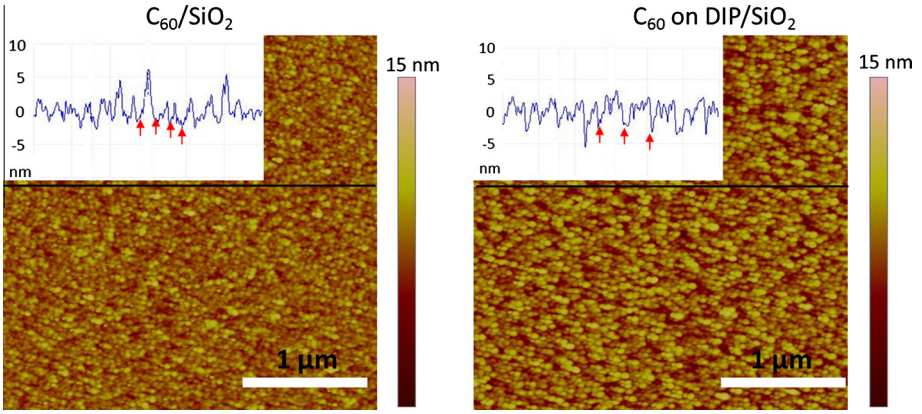

Fig. 4. AFM images (3 μm × 3 μm) of C_{60} films grown on (a) SiO_2 and (b) DIP/SiO_2. Inset in each figure shows line shape morphology along the black line.

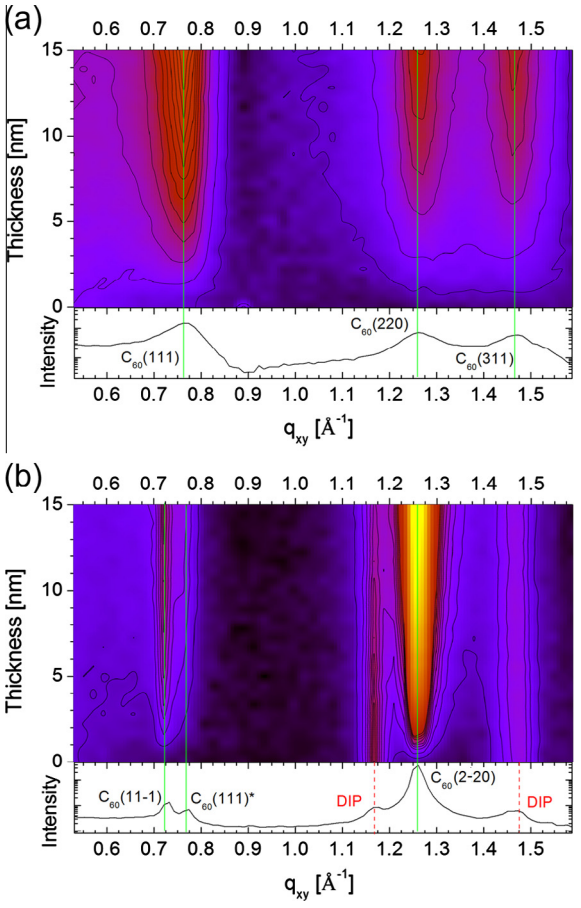

Fig. 5. Thickness dependent in-plane GIXD data from C_{60} films grown on (a) SiO_2 and (b) DIP/SiO_2. At the bottom of each image a GIXD scan at the final thickness (15 nm) with peak assignments are shown. Note that peak assignments for both samples vary, since in contrast to the randomly oriented C_{60} domains on SiO_2 the C_{60} domains on DIP are textured to (111) orientation [23]. Randomly oriented domains exist very slightly also in the C_{60} on DIP as denoted by the $(111)^*$ reflection in (b).

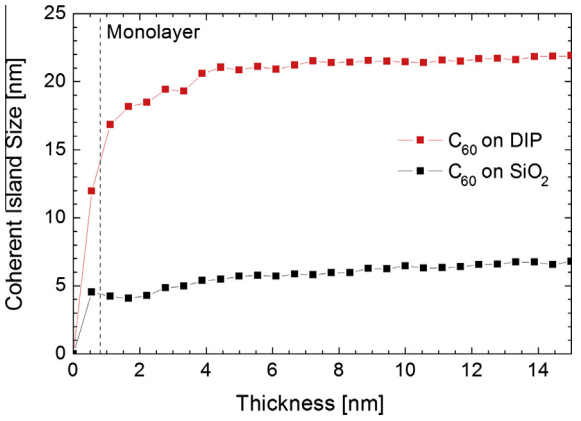

Fig. 6. In-plane coherent island sizes l_s derived from the real-time GIXD data in Fig. 5. The vertical broken line indicates the nominal thickness of one complete C_{60} layer.

mean free path [29,35]. The UPS spectrum of C_{60}/SiO_2 clearly shows deep trap states at a binding energy of 0.8–1.7 eV (the HOMO peak of C_{60} is located at 2.6 eV). After 3-nm-thick DIP modification of SiO_2, the HOMO spectrum of C_{60} shifts to higher binding energies (at 2.75 eV), indicating the E_F moves closer to the LUMO as observed previously [22]. This E_F shift suggests rapider decrease in the contribution of LUMO (3-hold degeneracies)-originated gap states than that of HOMO (5-hold degeneracies)-originated gap states. Furthermore an apparent decrease in the HOMO-related gap states can be seen in the spectrum of C_{60} on DIP/SiO_2. These results on the HOMO position and the DOGS demonstrate that the DIP-template layer can reduce significantly the density of trap states in the C_{60} film both for occupied and unoccupied states. Considering the existing trap states in organic films, which originally due to tiny disorder in both crystal-grains and their boundaries [29], the DIP-template layer acts not only for passivating traps at the SiO_2 surface, but also for increasing C_{60} crystallinity and orientation of crystal grains, and thus for dramatic decrease in trap states in C_{60} films.

The improved device stability suggests that the structure of DIP-template layer and thus C_{60} over layer is durable during device operation. Moreover, as demonstrated in Fig. 2a, the sub-threshold swing slope for the DIP-template OTFT is much larger than that for the DIP-free one [38].

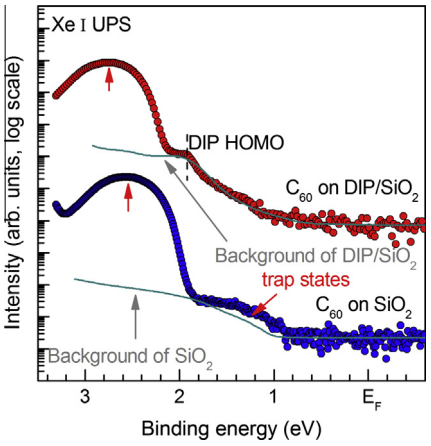

Fig. 7. Xe I UPS log scale spectra of the C_{60}/(~15 nm)/SiO_2 and C_{60} (~15 nm)/DIP (~3 nm)/SiO_2 thin films in C_{60}-HOMO binding energy region. The background of the SiO_2 and DIP modified SiO_2 substrates (dark cyan color) are also shown. Due to a tiny electron exchange and/or the molecular polarization at the interface [39], the DIP spectrum was shifted by 0.39 eV to lower binding energy side to fit the DIP background of C_{60}/DIP/SiO_2 spectra. Both the DIP/SiO_2 and SiO_2 spectra were rescaled in order to fit the background of C_{60} spectra. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

This also indicates the much lower density of electron shallow trap states in the case of using DIP template layer. Considering the decreased trap states in the binding energy region of 0.8–1.7 eV in DIP-template C_{60} films, the UPS results also suggest a reduction in shallow trap states, since the shallow and deep trap states are changed together [9], which are consistent with the device performance. For further understanding of the device property, we need computational studies of the energy distribution and the value of DOGS by considering spatial distributions of HOMO and LUMO and their state degeneracies.

4. Conclusion

In conclusion, C_{60}-based OTFTs with high μ_n and high operational stability are achieved by employing ultrathin DIP as a template layer to grow (111) oriented C_{60} film with better crystallinity. Improved μ_n can reach 2.92 $cm^2\,V^{-1}\,s^{-1}$, which is over one order of magnitude higher compared with μ_n in the reference device without DIP. Real-time GIXD, AFM images and UPS spectra indicate that the inserted DIP layer does not only improve the quality of the C_{60} active layer on top, but also modifies the C_{60}/dielectric interface to decrease significantly the density of trap states in the C_{60}-based OTFT. The two effects contribute to the drastic improvements of μ_n and operational stability in the C_{60}-based OTFTs. More improvement could be expected by optimizing, for example, the electrode-organic semiconductor interface that also influences structure imperfection of organic semiconductor films.

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